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EXAMINER

SONG, JASMINE

ART UNIT PAPER NUMBER

2188

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/372,296

Applicant(s)

KUCH ET AL.

Examiner

Jasmine Song

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 30 July 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_ 6) ☐ Other: \_\_\_\_

## **Detailed Action**

1. This office action is in response to the amendment C filed on 07/30/2002.

## **Specification**

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## **Drawings**

3. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 07/30/2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

## **Claim Rejections - 35 USC § 112**

4. The rejection of claim 8 under 35 USC § 112, second paragraph has been **withdrawn** due to amendment.

### **Claim Rejections - 35 USC § 102**

5. The rejection of claims 1,4-5,8 and 15 under 35 U.S.C. 102(e) and the rejection of claims 2-3,9-12 and 16-19 under 35 U.S.C. 103(a) are maintained but updated to show the amendment. The rejection of claims 6-7,13-14 and 20-21 under 35 U.S.C. 103(a) as being unpatentable over Greiner is also maintained.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 1,4-5,8 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Greiner et al., U.S. Patent 6216208.

Regarding claim 1, 8 and 15, Greiner et al. teach a system comprising:

a memory is taught as external memory (col.2, lines 15-16 and lines 56);

a bus is taught as the memory bus or CPU bus(Fig. 1, element 300); and

a bus access circuit (Fig.1, element 100) coupled to the memory and the bus (Fig.1) to reduce latency in accessing the memory from the bus, the circuit comprising:

a pre-fetcher (Fig.1, prefetch queue) to pre-fetch a plurality of data from the memory (external memory) to a data queue (Fig.1, element 120) in response to a request (col.2, lines 59 to col.3, lines 10), and

a queue controller is taught as a cache controller coupled to the data queue (Fig.1, element 120) and the pre-fetcher to deliver the pre-fetched data (the prefetched data stored in the 120) from the data queue to a bus (CPU bus) independently of the memory (external memory)(col.5, lines 46-58).

Regarding claim 4, Greiner et al. teach that determining if the request is valid and processing a cache miss request if the request results in a cache miss is taught as the internal queue monitors the requests issued by the arbiter, and monitors data held by the cache to determine whether a copy of the requested location is held in the cache (col.2, lines 54-62).

Regarding claim 5, Greiner et al. teach that the processing of the cache miss request comprises: Providing a purge signal, marking an entry in a scheduler according to the purge signal; purging data corresponding to the marked entry (Fig.3,step 1030-1070-1090 and col.5, lines 7-17); and placing the request to the memory controller (col.5, lines 37-49).

### **Claim Rejections - 35 USC § 103**

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 2-3, 9-12 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greiner et al., U.S. Patent 6216208, in view of Kasper, U.S. Patent 6356962.

Regarding claim 2, 9 and 16, Greiner et al. teach the claimed invention (claims 1, 8 and 15) and the request causes the memory controller transferring the plurality of data to the data queue (col.2, lines 59 to col.3, lines 32), the request being buffered in a request queue (Fig.1, element 130 and col.2, lines 37-38).

Greiner does not teach that a watermark monitor is used to determine if an amount of data in the data queue is above a predetermined level, if not, the request causing the memory controller to transfer the plurality of data to the data queue.

However, Kasper teaches that a watermark is used to determine if an amount of data in the data queue is above a predetermined level, if not, the request causing the memory controller to transfer the plurality of data to the data queue (col.4, lines 7-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a watermark monitor to indicate that sufficient storage exists in the FIFO memory to receive additional data as taught by Kasper in the Greiner's system because it effectively increases bus and memory resource utilization (col.3, lines 35-42 and col.1, lines 9-11).

Therefore, one having ordinary skill in the art at the time the invention was made would have been motivated to provide a watermark monitor in the Greiner's system

because it would provide a “window” into the FIFO memory (col.3, lines 52-53) allowing the controller to transfer the data to the FIFO memory.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claims 3,10 and 17, Greiner et al. teach transferring the data from the data queue to the bus if the data in the data queue are ready. It is obvious that the data are transferred when the data are ready because the data must be ready before they are transferred (col.5, lines 46-58).

Regarding claims 11 and 18, Greiner et al. teach a peripheral bus controller (Fig.1, element 110) coupled to the bus (Fig.1, the line connected 110 and 130) and the pre-fetcher (Fig.1, element 160) to determine if the request is valid (col.2, lines 54-62);

a data coherence controller (Fig.2, element 170) coupled to the pre-fetcher to provide a purge signal (a buffer entry pointed by a pointer, col.5, lines 7-17) when the request corresponds to a cache miss (col.5, lines 7-17 and col.2, lines 54-62); and

a scheduler (Fig.2, element 110) coupled to the request queue (Fig.1, element 130) and the data coherence controller (Fig.2, element 170) to store entries corresponding to the requests, the entries being marked according to the purge signal from the data coherence controller (Fig.3,step 1030-1070-1090 and col.5, lines 7-17).

Regarding claims 12 and 19, Greiner et al. teach processing the cache miss request comprises:

a data mover (Fig.1, element 140) coupled to the data queue and the scheduler to transfer data from the memory to the data queue (col.2, lines 59 to col.3, lines 32), the data mover purging data corresponding to a marked entry from the scheduler (Fig.3, step 1030-1070-1090 and col.5, lines 7-17);

10. Claim 6-7, 13-14 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greiner et al., U.S. Patent 6216208 B1.

Regarding claims 6, 13 and 20, Greiner teaches the claimed independent claims as noted above. Greiner does not teach that the bus is a peripheral component interconnect bus (PCI bus). Official notice is taken that it is well known in the art that PCI bus is one of the most widely used types of buses. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use PCI bus in Greiner's bus system because PCI bus is an industry standard bus.

Regarding claims 7, 14 and 21, Greiner teaches the claimed independent claims as noted above. Greiner does not teach that the request is one of a 32-byte and a 64-byte requests. It is well known in the art that 32-byte or 64-byte data request is commonly used. It is also an obvious matter of design choice to use one of a 32-byte and 64-byte requests in Greiner's requested data, since these are power of 2.



### **Response to applicant's Arguments**

11. Applicant's arguments filed 07/30/2002 have been fully considered but they are not persuasive.

12. In response to applicant's argument that Greiner does not expressly or inherently disclose that a prefetcher to prefetch data from a memory to a data queue and a queue controller to deliver the prefetched data from the data queue to a bus independently of the memory, the Examiner recognizes that the above limitation is disclosed in the Greiner's reference. Greiner teaches that a prefetch queue 160 in communication with the internal queue 130 and the internal queue monitors the requests issued by the arbiter 110 (Fig.1) and informs the prefetch queue of read requests. The read requests may be requests for either instruction data or variable data to be read to the core 200, the read requests identify a memory address from which data is to be read. Over time, read request may exhibit a pattern indicating that the processor core is reading from sequential locations in external memory, when this pattern arise, the prefetch queue prefetches from the next location in the sequence and submits an address to the arbiter over data line 110e. The arbiter 110 is provided with circuitry that interprets the address as a prefetch request and generates a request code representing an instruction for a read of data to the cache (Fig.1, col.2, lines 59 to col.3, lines 10). When the internal queue identifies another read request identifying location, the data from that location will have been prefetched into the cache120, thus, the data may be delivered to the core

without resorting to the slower external bus (col.5, lines 54-58). Basically, Greiner teaches that the core issues the read requests, the internal queue monitors the read requests and inform the prefetch queue, the prefetch queue prefetches the memory addresses of the external memory if there is a indication that the processor is reading from the sequential address and the data associated with the memory addresses will send to the cahce, so when the processor core requests the data from those addresses, it only needs to access cache instead of accessing the external memory.

13. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a watermark monitor to indicate that sufficient storage exists in the FIFO memory to receive additional data as taught by Kasper in the Greiner's system because it effectively increases bus and memory resource utilization as stated above (col.3, lines 35-42 and col.1, lines 9-11 in Kasper's reference).

14. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

### Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

17. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do H. Yoo can be reached on 703-308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Application/Control Number: 09/372,295  
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Jasmine Song  
Patent Examiner



*Reginald G. Bragdon*  
REGINALD G. BRAGDON  
PRIMARY EXAMINER

October 17, 2002

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IMPORTANT NOTICE

The Examiner's art unit number has changed from 2187 to 2188 due to the recent realignment of workgroup 2180. Please use art unit 2188 on all correspondence related to this case.

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